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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/076,143	02/15/2002	Shinobu Torikoshi	62807-038	8856

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MCDERMOTT WILL & EMERY LLP
600 13TH STREET, N.W.
WASHINGTON, DC 20005-3096

EXAMINER	
CHOWDHURY, NIGAR	
ART UNIT	PAPER NUMBER
2621	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/076,143	TORIKOSHI ET AL.	
	Examiner	Art Unit	
	Nigar Chowdhury	2621	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 September 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *22-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *22-27,30,31,33,34 and 37* is/are allowed.

6)☒ Claim(s) *28,29,32,35,36 and 38-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/12/2005,2/15/2002*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 28, 29, 32, 35, 36, and 42 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 6,108,485 by Kim.

2. Regarding **claim 28**, a decoder for processing an input audio signal associated with time information for synchronization in accord with a reference clock outputted from a clock generator for generating the reference clock independent of the time information for synchronization and outputting the processed audio signal (Fig. 3-4, Col. 2 lines 24-Col. 4 lines 46, Col. 5 lines 56-Col. 7 lines 67), comprising:

- A frequency dividing unit, responsive to the clock generator, for forming a frame sync signal for output on the basis of the reference clock
- An audio signal processing unit, responsive to the frequency dividing unit, for executing a sampling transforming process of the input audio signal by

setting the number of samples of one frame period in which the frame sync signal for output is used as a reference to the number of samples of one frame.

3. Regarding **claim 29**, a DV decoder for processing a input video signal and an input audio signal associated with time information for synchronization in accord with a reference clock outputted from a clock generator for generating the reference clock independent of the time information for synchronization and outputting the processed video and audio signals, comprising: (Fig. 3-4, Col. 2 lines 24-Col. 4 lines 46, Col. 5 lines 56-Col. 7 lines 67)

- A frequency dividing unit, responsive to the clock generator, for forming a frame sync signal for output on the basis of the reference clock
- A video signal processing unit, responsive to the frequency dividing unit, for processing the input video signal and outputting the processed video signal synchronized with the frame sync signal for output
- An audio signal processing unit, responsive to the frequency dividing unit, for executing a sampling transforming process of the input audio signal so that a number of samples of one frame period in which the frame sync signal for output is used as a reference is equal to the predetermined number of samples.

4. Regarding **claim 32**, a DV decoder for processing an input digital signal including video signal, an audio signal and an input side frame sync signal in accord with a reference clock outputted from a clock generator for generating the reference clock independent of the input side frame sync signal and for outputting the processed video and audio signals, comprising: (Fig. 3-4, Col. 2 lines 24-Col. 4 lines 46, Col. 5 lines 56-Col. 7 lines 67)

- A frequency dividing unit, responsive to the clock generator, for forming a frame sync signal for output and a clock enable signal for an input process on the basis of the reference clock
- An input processing unit, responsive to the frequency dividing unit, for separating and outputting the video signal, the audio signal, and the input side frame sync signal from the input digital signal in response to the clock enable signal for the input process which is outputted from the frequency dividing unit
- A video processing unit, responsive to the frequency dividing unit, for processing the video signal which is outputted from the input processing unit and forming the video signal synchronized with the fi'ame sync signal for output
- An audio signal processing unit, responsive to the frequency dividing unit, for executing a sampling transforming process to the audio signal from the input processing unit so that a number of samples of one frame period

in which the frame sync signal for output is used as a reference equals to a predetermined number of samples.

5. Regarding **claim 35**, a decoder wherein the input audio signal is a signal in an unlocked mode in a DV standard, and the audio processing unit transforms the number of samples into a number of samples which has been predetermined in a locked mode in the DV standard (Col. 3 lines 67-Col. 4 lines 18).

6. Regarding **claim 36**, a DV decoder wherein the input audio signal is a signal in an unlocked mode in a DV standard, and the audio processing unit transforms a number of samples into the number of samples which has been predetermined in a locked mode in the DV standard (Col. 3 lines 67-Col. 4 lines 18).

7. Regarding **claim 42**, a signal processing method for processing DV data including an input video signal and an input audio signal in accord with a reference clock which is asynchronous with time information for synchronization contained in the DV data, comprising the steps of: (Fig. 3-4, Col. 2 lines 24-Col. 4 lines 46, Col. 5 lines 56-Col. 7 lines 67)

- Inputting the video signal and the audio signal
- Synchronizing the input video signal on a frame unit basis in response to the reference clock

- Outputting the video signal which was synchronized on the frame unit basis
- Sampling transforming the input audio signal in response to the reference clock on a frame unit basis different from the time information for synchronization
- Outputting the audio signal which was sampling transformed.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 38-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,108,485 by Kim.

9. Regarding **claim 38**, Kim discloses a recording device Comprising: (Fig. 3-4, Col. 2 lines 24-Col. 4 lines 46, Col. 5 lines 56-Col. 7 lines 67)

- A decoder for processing an input audio signal input with time information for synchronization in accord with a reference clock outputted from a clock generator for generating the reference clock independent of the time information for synchronization and outputting the processed audio signal, comprising:

- A frequency dividing unit, responsive to the clock generator, for forming a frame sync signal for output on the basis of the reference clock
- An audio signal processing unit, responsive to the frequency dividing unit, for executing a sampling transforming process of the input audio signal by setting the number of samples of one frame period in which the frame sync signal for output is used as a reference to the number of samples of one frame

- A recording unit

Kim fails to disclose MPEG compression. It is noted that the use of MPEG is old and well-known in the recording art. Therefore, official notice is taken. Moreover, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have a well-known MPEG compression for compressing the information to have more space in the storage medium.

10. Regarding **claim 39**, a recording device comprising:

- DV decoder for processing a input video signal and an input audio signal inputted with time information for synchronization in accord with a reference clock outputted from a clock generator for generating the reference clock independent of the time information for synchronization and outputting the processed video and audio signals, comprising:

- A frequency dividing unit, responsive to the clock generator, for forming a frame sync signal for output on the basis of the reference clock
- A video signal processing unit, responsive to the frequency dividing unit, for processing the input video signal and outputting the processed video signal synchronized with the frame sync signal for output
- An audio signal processing unit, responsive to the frequency dividing unit, for executing a sampling transforming process of the input audio signal so that a number of samples of one frame period in which the frame sync signal for output is used as a reference is equal to the predetermined number of samples

- A recording unit

Kim fails to disclose MPEG compression. It is noted that the use of MPEG is old and well-known in the recording art. Therefore, official notice is taken. Moreover, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have a well-known MPEG compression for compressing the information to have more space in the storage medium.

11. Claims 40-41 are rejected for the same reason as discussed in the corresponding claim 39 above.

Allowable Subject Matter

12. Claims 22-27, 30, 31, 33, 34, 37 are allowable.

The following is a statement of reasons for the indication of allowable subject matter: The independent claim 22 is identifies the uniquely distinct feature for "a video signal processing unit, responsive..... frequency dividing the reference clock",

The independent claim 24 is identifies the uniquely distinct feature for "a video signal processing unit, coupled..... and the input video signal",

The independent claim 30 is identifies the uniquely distinct feature for "a video processing unit, responsive.... Sync signal for output; and an audio processing unit, responsive.....inputted audio signal",

The independent claim 31 is identifies the uniquely distinct feature for "a video signal processing unit, coupled..... sync signal for output", "a sampling transform processor, coupled.....audio signal process",

The independent claim 33 is identifies the uniquely distinct feature for "a video processing unit, responsive.....frame sync signal for output"

Kim, 6,108,485 discloses an audio data playback clock signal generating apparatus of a digital VCR synchronizes an audio frame playback synchronization signal with a video frame synchronization signal when an audio data recorded in a magnetic tape is played back based on a phase error of an audio data frame size AF-SIZE and an audio data playback clock signal of the previous video frame. The audio

data playback clock signal generating apparatus comprises an audio data frame size decoder, a low pass filter, a voltage-controlled oscillator, and phase error generating block and can be implemented by a large scale integration (LSI) to thereby provide a non-complex circuit and an accurate synchronization between the audio frame playback synchronization signal and the video frame synchronization signal.

Poimboeuf, 5,764,965 discloses a synchronization backbone for use in a computer system having a system board containing at least one central processing unit for processing digital data, a memory coupled to the system board for storing the digital data, a plurality of subsystems, and a bus structure for transmitting electrical signals between the system board, the memory, and the plurality of subsystems. The synchronization backbone provides the infrastructure that enables professional quality synchronization between the various subsystems. A clock generator is used to generate a system clock that is transmitted to each of the subsystems. The sample rate of a designated subsystem is used as a digital synchronization signal

None of the prior art, either singularly or in combination, fails to anticipate or render the above underlined limitations obvious. Claims 23,25-27, 34, 37 are dependent on claims 22, 24, 31 and therefore also allowable.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nigar Chowdhury whose telephone number is 571-272-8890. The examiner can normally be reached on 9 AM - 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thai Tran can be reached on 571-272-7382. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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01/08/2007